IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A method for prefetching data in a multiprocessing computer system comprising:

a first cache receiving a request to access a first line of data, wherein the request to access the first line of data is a read request;

determining that a cache miss with respect to the first line occurred; and

transmitting a bundled transaction on a system interconnect in response to the cache miss, wherein the bundled transaction combines a request for the first line of data and a prefetch request, and wherein the bundled transaction includes a bit-map indicating selected lines of data beyond the first line to be prefetched in response to the prefetch request;

wherein, in response to the bundled transaction, the method further comprises:

determining that a second cache is an owner of the first line of data;

determining whether the second cache is also an owner for any of the selected lines of data beyond the first line;

the second cache transmitting to the first cache any of the selected lines for which the second cache is an owner; and

the second cache transmitting a null-data packet to the first cache for each of a remainder of the selected lines of data for which the second cache is not an owner.

2. (Cancelled)

3. (Currently Amended) The method as recited in claim ~~2~~ 1 wherein the prefetch request is a prefetch read request.

4. (Original) The method as recited in claim 3 wherein the prefetch read request is a request to a sequential cache line.

5 - 9. (Cancelled)

10. (Currently Amended) A multiprocessing computer system comprising:

a microprocessor configured to convey a request to access a first line of data, wherein the request to access the first line of data is a read request; ~~and~~

a first cache coupled to receive the request, wherein the first cache is configured to transmit a bundled transaction on a system interconnect in response to a cache miss, wherein the bundled transaction combines a request for the first line of data and a prefetch request, and wherein the bundled transaction includes a bit-map indicating selected lines of data beyond the first line to be prefetched in response to the prefetch request; and

a second cache, wherein in response to the bundled transaction and a determination that the second cache is an owner of the first line of data, the second cache is configured to transmit to the first cache any of the selected lines for which it is an owner and is configured to transmit a null data packet to the first cache for each of a remainder of the selected lines for which it is not an owner.

11. (Cancelled)

12. (Currently Amended) The multiprocessing computer system as recited in claim ~~11~~ 10 wherein the prefetch request is a prefetch read request.

13. (Original) The multiprocessing computer system as recited in claim 12 wherein the prefetch read request is a request to a sequential cache line.

14 -20. (Cancelled)